



欣瑞达液晶显示技术
X.R.D LCD TECHNOLOGY CO., LTD

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
MODEL	XRDG-G12864B2FDTGWSNN-10
CUSTOMER APPROVED	

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CONTENTS

- **MODULE CLASSIFICATION INFORMATION**
- **PHYSICAL DATA**
- **MECHANICAL DIMENSIONS**
- **BLOCK DIAGRAM**
- **INTERFACE PIN CONNECTIONS**
- **ABSOLUTE MAXIMUM RATINGS**
- **ELECTRICAL CHARACTERISTICS**
- **BACKLIGHT**
- **OPTICAL CHARACTERISTICS**
- **OPERATING PRINCIPLES & METHODS**
- **DISPLAY DATA RAM ADDRESS MAP**
- **POWER SUPPLY FOR LCM MODULE**
- **RELIABILITY**
- **INSPECTION CRITERIA**
- **PRECAUTIONS FOR USING LCD MODULES**
- **USING LCD MODULES**

■ MODULE CLASSIFICATION INFORMATION

X R D G - G 1 2 8 6 4 B 2 F D T G W S N N - 1 0

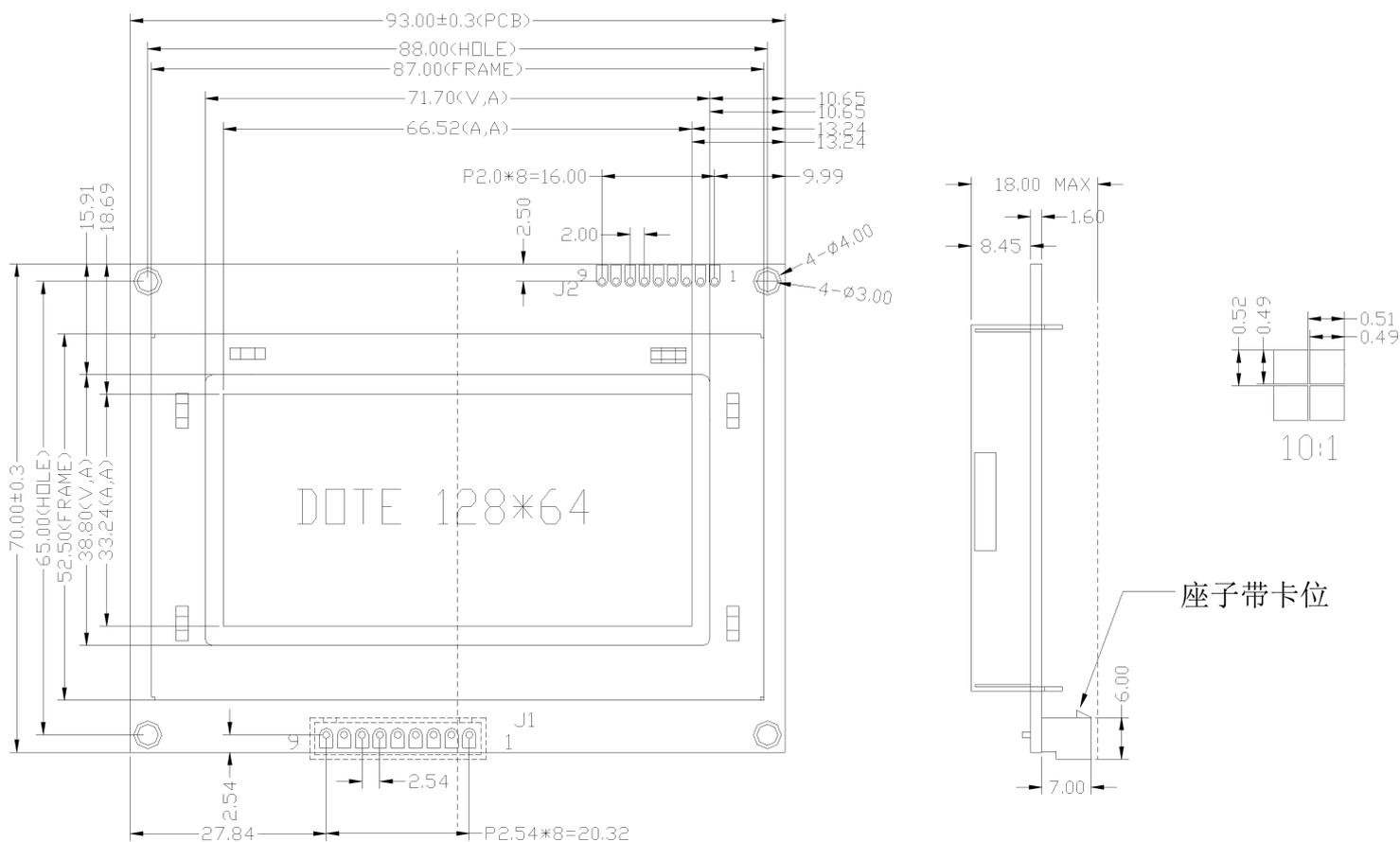


PRODUCT USAGE
 10:NO.10
 SPECIAL NEEDS
 N:NO SPECIAL NEEDS
 CHARACTERS OR FONT MODE
 N:WITHOUT
 TEMP.GRADE
 S:-20°-+70°
 BACKLIGHT MODE & COLOR
 W:WHITE
 POLARIZER COLOR
 G:GREY
 POLARIZER MODE
 T:TRANSMISSIVE
 VIEWING ANGLE
 D:6 0' CLOCK
 LCD TYPE
 F:FSTN
 MODEL SERIES
 B2
 DISPLAY FORMAT
 12864:128COLUMNS*64ROWS
 IC PACKING
 G:COG
 LCM TYPE
 G:GRAPHIC
 STANDARD MODULE

■ PHYSICAL DATA

ITEM	STANDARD VALUE	UNIT
NUMBER OF GRAPHIC	128×64	mm
MODULE DIMENSION	93.0×70.0×18.0(MAX)	mm
EFFECTIVE DISPLAY AREA	66.52*33.24	mm
DOT SIZE	0.49×0.49	mm
DOT PITCH	0.52×0.52	mm
LCD TYPE	FSTN/TRANSMISSIVE/GREY	
DUTY/BIAS	1/65 DUTY / 1/9 BIAS	
VIEWING DIRECTION	6	o'clock
BACK LIGHT TYPE	SIDE LIT LED	
BACK LIGHT COLOR	WHITE	
INTERFACE	SPI	
APPROX. WEIGHT	TBD	g

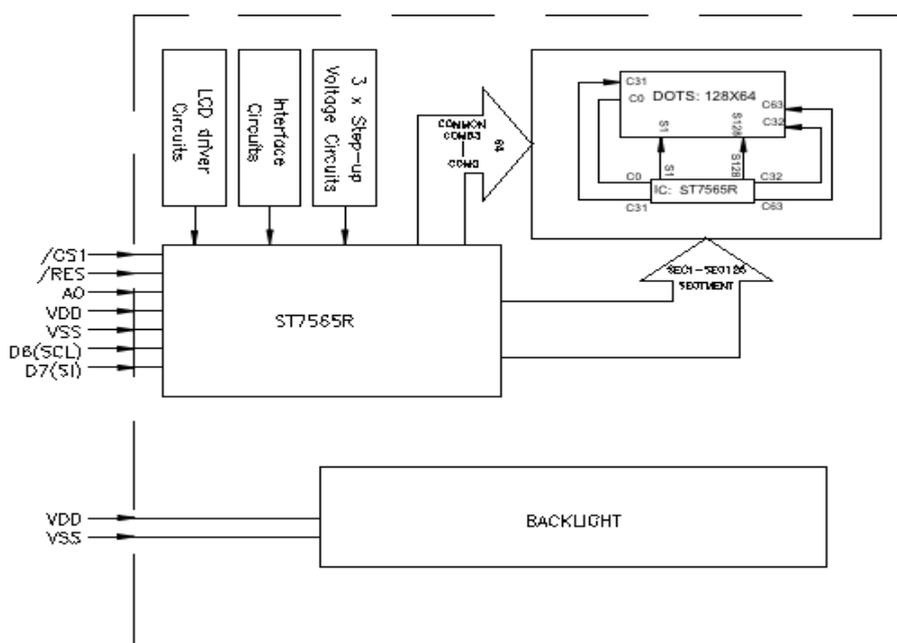
■ MECHANICAL DIMENSIONS



NOTES:

ALL UNMARKED TOLERANCES: ±0.2mm;

■ BLOCK DIAGRAM



■ INTERFACE PIN CONNECTIONS

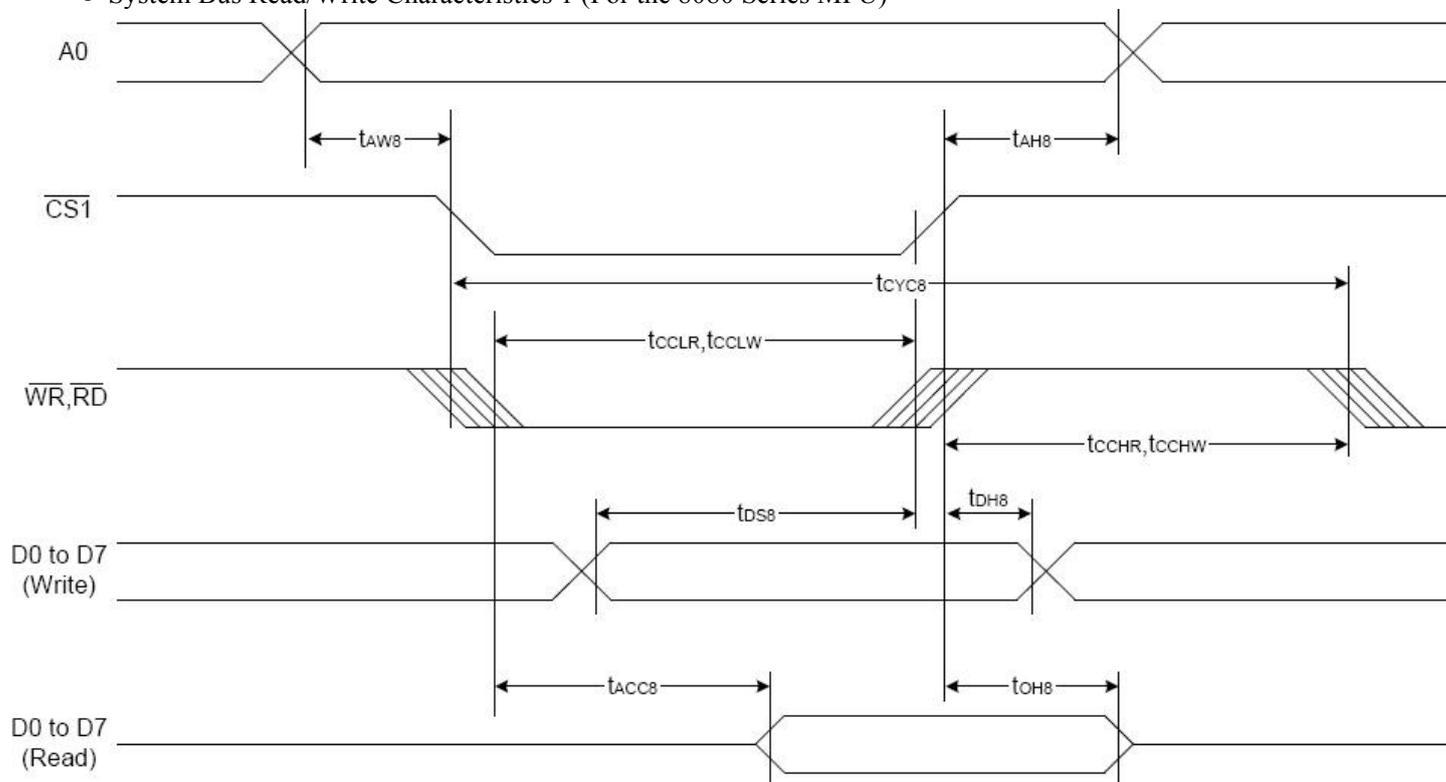
Interface: J1ANDJ2

NO	SYMBOL	LEVEL	FUNCTION
1	VSS	0V	Ground
2	VDD	3.3V	Power supply for logic circuit
3	RS	H/L	Register select input pin. LCD_RS= "H": DB0 to DB7 are display data. LCD_RS= "L": DB0 to DB7 are control data.
4	CLK	I	Serial clock input
5	SDA	I	Serial data input
6	/REST	L	Reset signal When LCD_RST is set to "L", the register settings are initialized. The reset operation is performed by the LCD_RS signal level.
7	/CS	I	This is the chip select signal. When /CS = "L", then the chip select becomes active and data/command I/O is enabled
8	LEDK		Back light cathode
9	LEDA		Back light anode

■ ELECTRICAL CHARACTERISTICS

▼ AC Characteristics

- System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)



(VDD = 3.3V, Ta = -20 to 70°C)

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Address hold time	A0	tAH8		0	--	ns
Address setup time		tAW8		0	--	
System cycle time		tCYC8		240	--	
Enable L pulse width (WRITE)	WR	tCCLW		80	--	
Enable H pulse width (WRITE)		tCCHW		80	--	
Enable L pulse width (READ)	RD	tCCLR		140	--	
Enable H pulse width (READ)		tCCHR		80	--	
WRITE Data setup time	D0-D7	tDS8		40	--	
WRITE Address hold time		tDH8		0	--	
READ access time		tACC8	CL=100pF	--	70	
READ Output disable time		tOH8	CL=100pF	5	50	

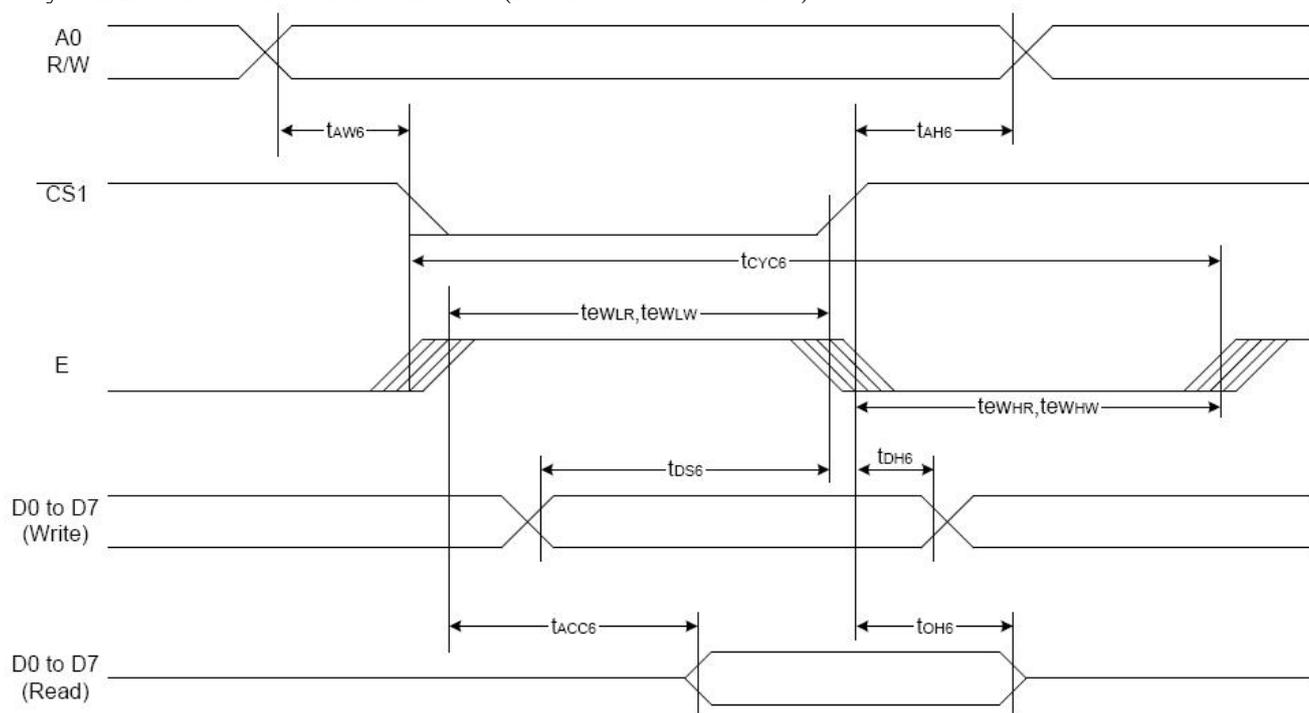
*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast,

$$(tr + tf) \leq (tCYC8 - tCCLW - tCCHW) \text{ for } (tr + tf) \leq (tCYC8 - tCCLR - tCCHR) \text{ are specified.}$$

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between /CS1 being "L" and /WR and /RD being at the "L" level.

● System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)



(VDD = 3.3V , Ta = -20 to 70°C)

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Address hold time	A0	tAH6		0	--	ns
Address setup time		tAW6		0	--	
System cycle time		tCYC6		240	--	
Enable L pulse width (WRITE)	E	tEWLW		80	--	
Enable H pulse width (WRITE)		tEWHW		80	--	
Enable L pulse width (READ)	RD	tEWLR		80	--	
Enable H pulse width (READ)		tEWHR		140	--	
WRITE Data setup time	D0-D7	tDS6		40	--	
WRITE Address hold time		tDH6		0	--	
READ access time		tACC6	CL=100pF	--	70	
READ Output disable time	tOH6	CL=100pF		5	50	

(VDD = 2.7V , Ta = -20 to 70°C)

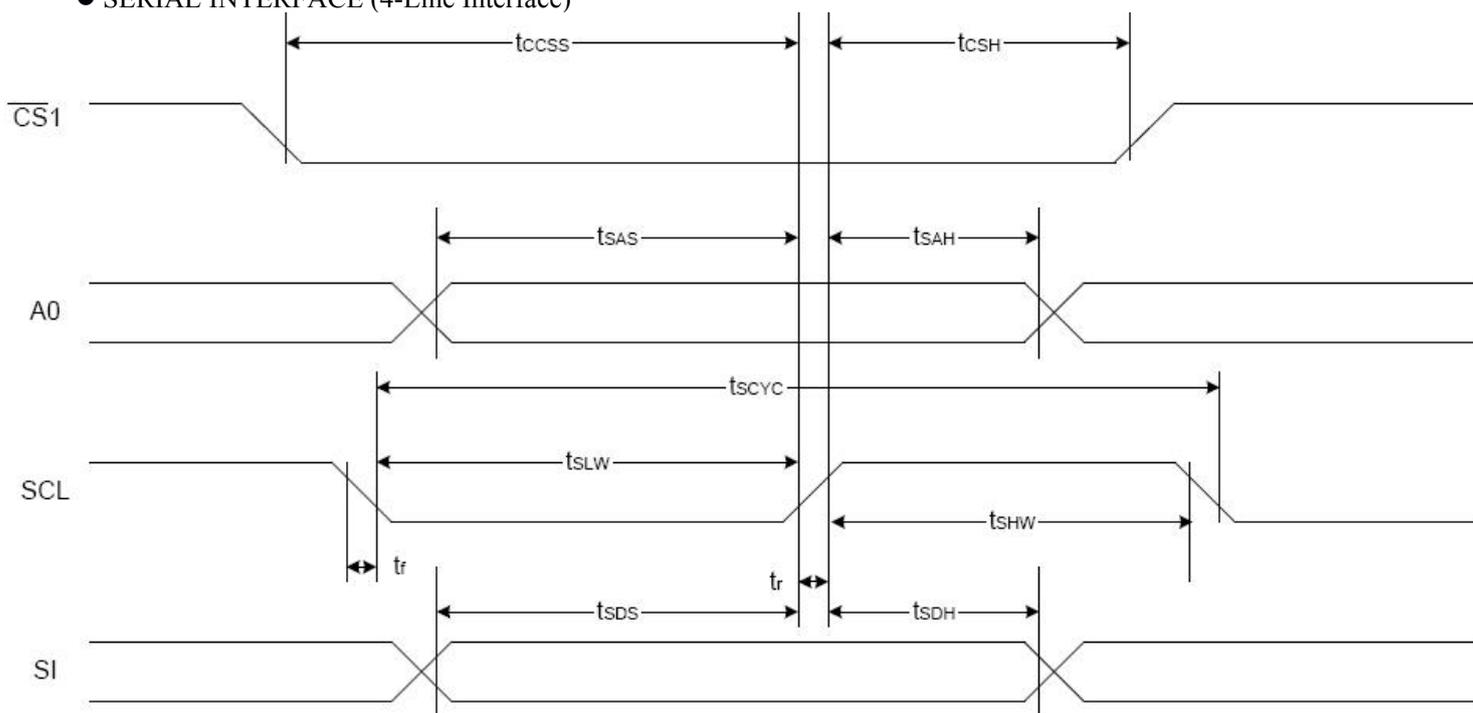
Parameter	Signal	Symbol	Condition	Min	Max	Unit
Address hold time	A0	tAH6		0	--	ns
Address setup time		tAW6		0	--	
System cycle time		tCYC6		400	--	
Enable L pulse width (WRITE)	E	tEWLW		220	--	
Enable H pulse width (WRITE)		tEWHW		180	--	
Enable L pulse width (READ)	RD	tEWLR		220	--	
Enable H pulse width (READ)		tEWHR		180	--	
WRITE Data setup time	D0-D7	tDS6		40	--	
WRITE Address hold time		tDH6		0	--	
READ access time		tACC6	CL=100pF	--	140	
READ Output disable time	tOH6	CL=100pF		10	100	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≤(tCYC6 - tEWLW - tEWHW) for (tr + tf) ≤(tCYC6 - tEWLR - tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between /CS1 being "L" and E.

● SERIAL INTERFACE (4-Line Interface)



(VDD = 3.3V , Ta = -20 to 70°C)

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Serial Clock Period		tSCYC		50		ns
SCL "H" pulse width	SCL	tSHW		25		
SCL "L" pulse width	SCL	tSLW		25		
Address setup time	A0	tSAS		20		
Address hold time	A0	tSAH		10		
Data setup time	SI	tSDS		20		
Data hold time	SI	tSDH		10		
CS-SCL time	/CS1	tCSS		20		
CS-SCL time	/CS1	tCSH		40		

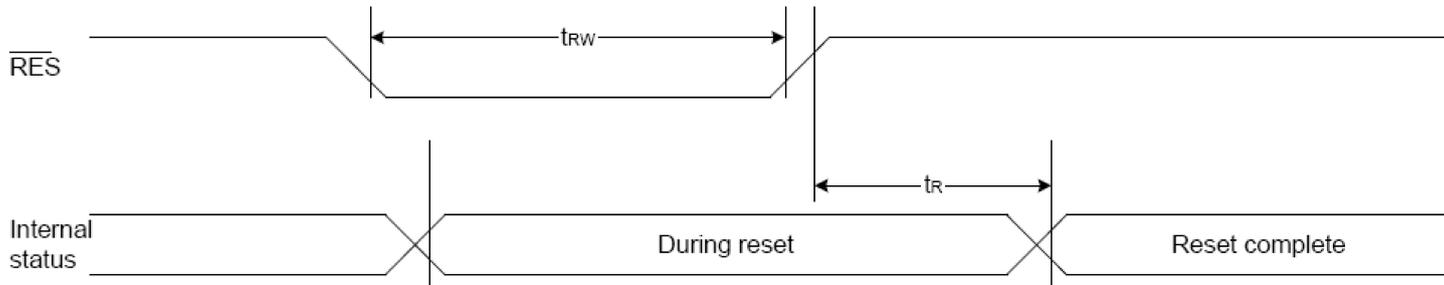
(VDD = 2.7V , Ta = -20 to 70°C)

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Serial Clock Period		tSCYC		100		ns
SCL "H" pulse width	SCL	tSHW		50		
SCL "L" pulse width	SCL	tSLW		50		
Address setup time	A0	tSAS		30		
Address hold time	A0	tSAH		20		
Data setup time	SI	tSDS		30		
Data hold time	SI	tSDH		20		
CS-SCL time	/CS1	tCSS		30		
CS-SCL time	/CS1	tCSH		60		

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

● RESET TIMING



(VDD = 3.3V , Ta = -20 to 70°C)

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Reset time		tR	---	---	1.0	us
Reset "L" pulse width	/RES	tRW	---	1.0	---	

(VDD = 2.7V , Ta = -20 to 70°C)

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Reset time		tR	---	---	2.0	us
Reset "L" pulse width	/RES	tRW	---	2.0	---	

*1 All timing is specified with 20% and 80% of VDD as the standard.

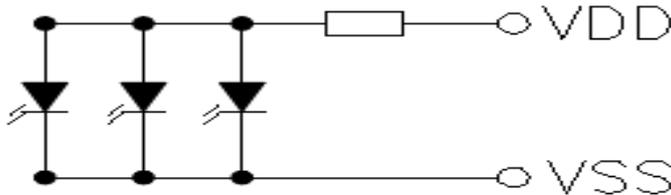
■ BACKLIGHT

▼ Backlight Type

Backlight Type: LED (WHITE)

▼ Power Supply For Backlight

(LED Chip 1*3=3dies)



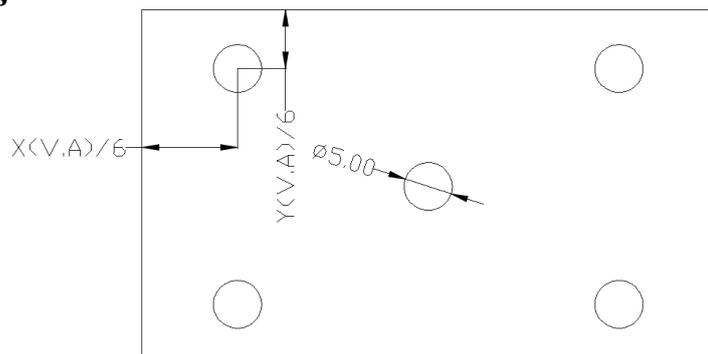
▼ Absolute Maximum Rating

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE	TEMPERATURE: 0°C ~ 70°C OPERATING CURRENT: 100mA/100%	0.0	5.0	5.0	V
LED CURRENT	I	0.00	0.00	0.00	
	P	0.00	0.00	0.00	
OPERATING	OPERATING VOLTAGE: 5.0V/100% OPERATING CURRENT: 100mA/100%	0.00	100		mA
OPERATING PULSE CURRENT	OPERATING VOLTAGE: 5.0V/100% OPERATING CURRENT: 100mA/100%	100		100	mA
OPERATING CURRENT		100		100	mA
LED LIFETIME	TEMPERATURE: 0°C ~ 70°C OPERATING CURRENT: 100mA/100%	10000			h

Note: For operation above 25°C, Then Ifm Ifp must be decreased, the Current decreased is -1.08mA/°C for DC drive and -2.58mA/°C Pulse drive, the power dissipation is -4.5mW/°C. The product working current must not more than the 70% of the Ifm or Ifp according to the working temperature.

▼ Electrical-Optical Characteristics

Note: The Master Screen's luminance is the average value of 5 points, and The $L_{vmin.}/L_{vmax.}$ is not less than 70%. The measurement instrument is BM-7 luminance Colorimeter. The aperture is $\Phi 5$ mm.



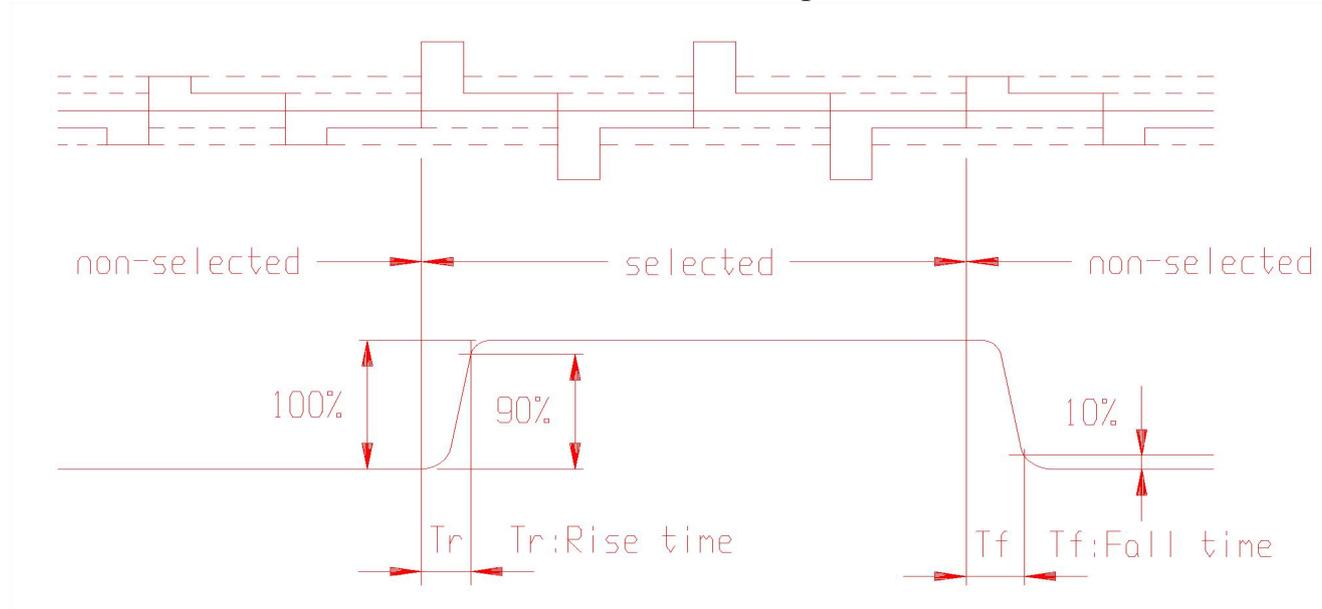
OPTICAL CHARACTERISTICS

Test instrument is LCD-5000, made in Japan

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks	Note
Operating voltage	Vop	25°C	9.8	10.0	10.2	V	---	---
Response time	Tr	25°C	---	66	250	ms	$\theta=0^\circ$	1
		0°C		950	1150	ms	$\Phi=0^\circ$	1
	Td	25°C	---	150	250	ms	$\theta=0^\circ$	1
		0°C		950	1150	ms	$\Phi=0^\circ$	1
Contrast ratio	Cr	25°C	2.0	6.5	---	---	$\theta=0^\circ$ $\Phi=0^\circ$	2
Viewing angle range	θ	$Cr \geq 2$	---	45	---	deg	$\theta=0^\circ$	3
			---	30	---	deg	$\theta=180^\circ$	3

Definition Of Viewing Angle

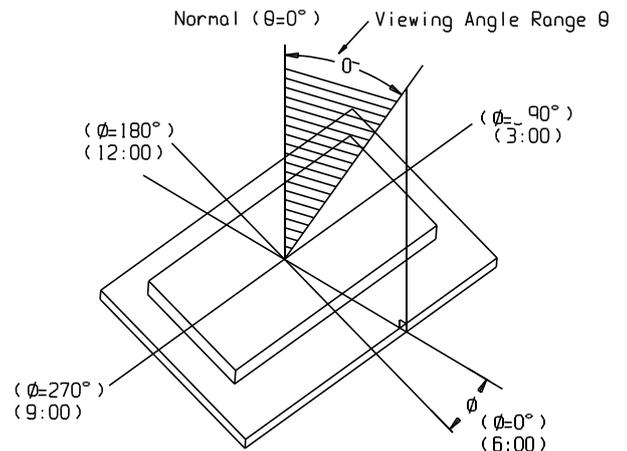
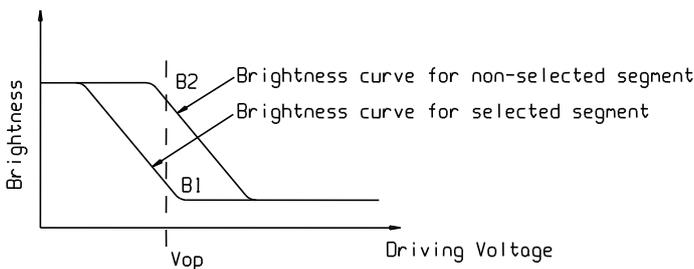
Note1: Definition of response time



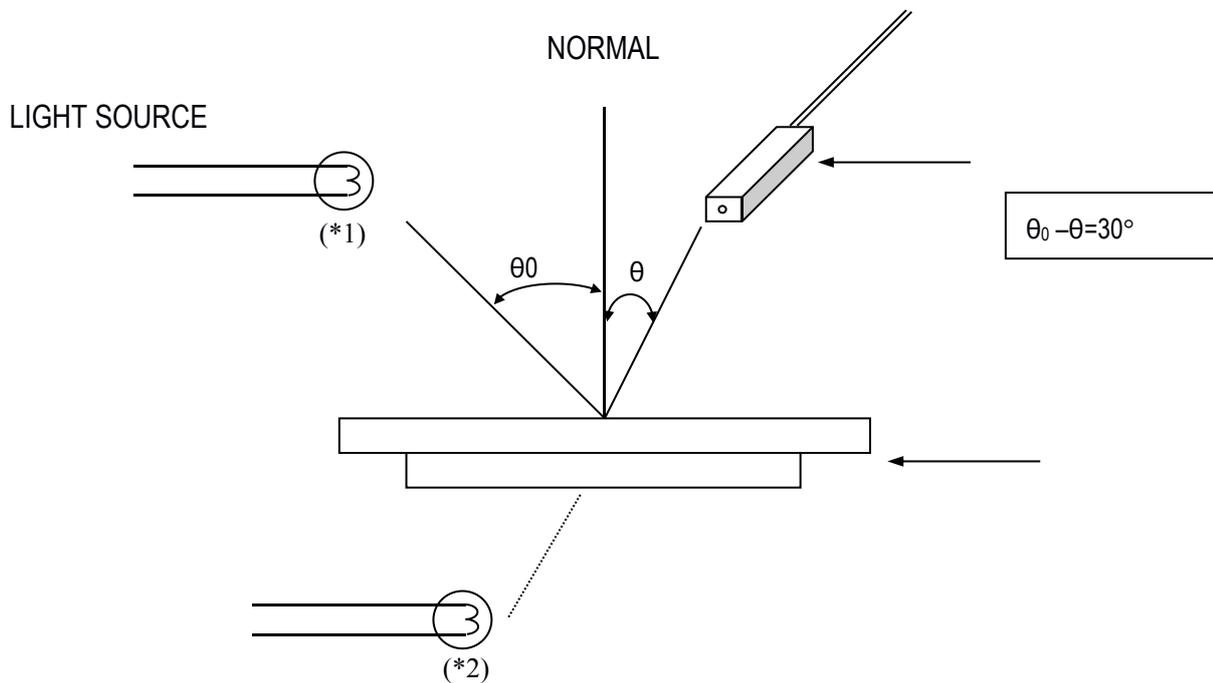
Note2: Definition of contrast ratio 'Cr'

Note3: Definition of viewing angle range ' θ '

$$Cr = \frac{\text{Brightness of non-selected segment}(B2)}{\text{Brightness of selected segment}(B1)}$$



Note4:Measuring Instruments For Electro-optical Characteristics



*1.Light source position for measuring the reflective type of LCD panel

*2.Light source position for measuring the transfective / transmissive types of LCD panel

■ OPERATING PRINCIPLES & METHODS

▼ MICROPROCESSOR INTERFACE

● Selecting Parallel / Serial Interface

This product has five types of interface with an MPU, which are two parallel and one serial interfaces.

Interface type	/CS1	A0	/RD (E)	/WR (R/W)	D0-D5	D6(SCL)	D7(SI)
80 serial 8-bit parallel	/CS1	A0	/RD	/WR	D0-D5	D6	D7
68 serial 8-bit parallel	/CS1	A0	E	R/W	D0-D5	D6	D7
4 line SPI mode	/CS1	A0	--	--	--	SCL	SI

Note: "--" means "disabled" in pins A0, E_RD, and RW_WR, and "high impedance" in pins DB0 to DB5

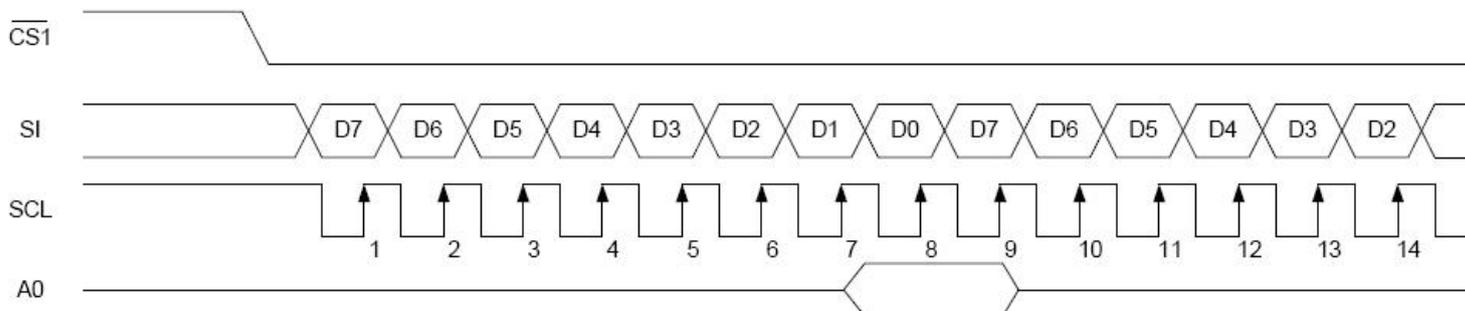
● Parallel Interface

The product identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) as shown in table:

Common	6800-series		8080-series		Description
A0	R/W	E	/RD	/WR	
H	H	H	L	H	Display data read out
H	L	H	H	L	Display data write
L	H	H	L	H	Register status read
L	L	H	H	L	Writes to internal register (instruction)

● The 4-line SPI Interface

When the 4-line SPI interface has been selected then when the chip is in active state (/CS1 = "L") the 4-line SPI data input (SI) and the 4-line SPI clock input (SCL) can be received. The 4-line SPI data is read from the 4-line SPI data input pin in the rising edge of the 4-line SPI clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth 4-line SPI clock for the processing. The A0 input is used to determine whether or the 4-line SPI data input is display data or command data; when A0 = "H", the data is display data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the 4-line SPI clock after the chip becomes active.



* When the chip is not active, the shift registers and the counter are reset to their initial states.

* Reading is not possible while in 4-line SPI interface mode.

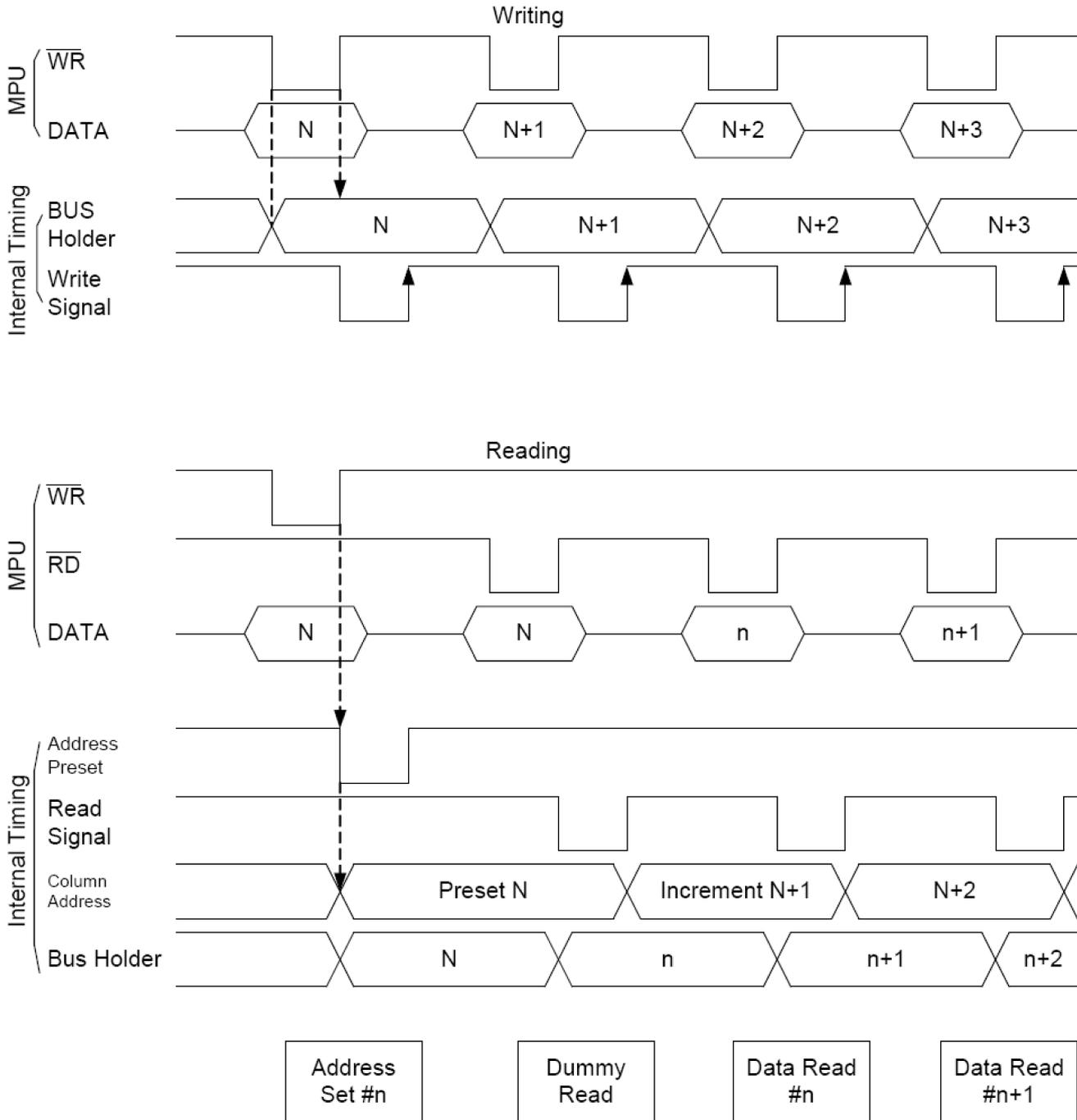
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

● The Chip Select

The product has one chip select terminals: /CS1. The MPU interface or the 4-line SPI interface is enabled only when /CS1 = "L". When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, /RD, and /W R inputs are inactive. When the 4-line SPI interface is selected, the shift register and the counter are reset

● The Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (tCYC) requirement alone in accessing the Product. Wait time may not be considered. And, in the Product, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus. Internal data bus, For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle. There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted. This relationship is shown in Figure

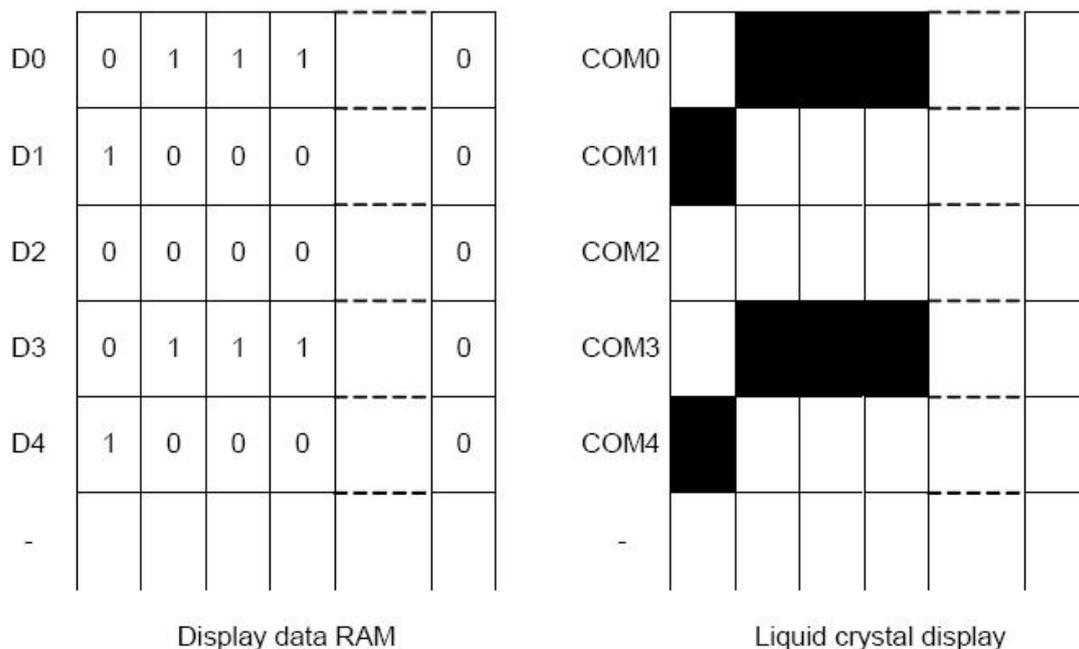


● **The Busy Flag**

When the busy flag is “1” it indicates that the product is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time, (tCYC) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

● **Display Data RAM**

The display data RAM stores the dot data for the LCD. It has a 65 (8 page x 8 bit +1) x 132 bit structure. As is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the LCD display common direction; there are few constraints at the time of display data transfer when multiple product are used, thus and display structures can be created easily and with a high degree of freedom, Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).



● The Page Address Circuit

Page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access, Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is a special RAM for icons, and only display data D0 is used.

● The Column Addresses

The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the incrementing of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to respect both the page address and the column address. Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized. As is shown in Figure

SEG Output ADC	SEG0	SEG127	SEG128	SEG129	SEG130	SEG131
(D0) "0"	0	→Column Address→ 127	128	129	130	131
(D0) "1"	131	←Column Address← 4	3	2	1	0

● The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output, for PRODUCT, the detail is shown page.11) The display area is a 65 line area for the product.

If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

Page Address				Data		Line Address	When the common output is normal	COM Output
D3	D2	D1	D0					
0	0	0	0	D0	Page 0	00H	48 lines	COM0
				D1		01H		COM1
				D2		02H		COM2
				D3		03H		COM3
				D4		04H		COM4
				D5		05H		COM5
				D6		06H		COM6
				D7		07H		COM7
0	0	0	1	D0	Page 1	08H	52 lines	COM8
				D1		09H		COM9
				D2		0AH		COM10
				D3		0BH		COM11
				D4		0CH		COM12
				D5		0DH		COM13
				D6		0EH		COM14
				D7		0FH		COM15
0	0	1	0	D0	Page 2	10H	64 lines	COM16
				D1		11H		COM17
				D2		12H		COM18
				D3		13H		COM19
				D4		14H		COM20
				D5		15H		COM21
				D6		16H		COM22
				D7		17H		COM23
0	0	1	1	D0	Page 3	18H	54 lines	COM24
				D1		19H		COM25
				D2		1AH		COM26
				D3		1BH		COM27
				D4		1CH		COM28
				D5		1DH		COM29
				D6		1EH		COM30
				D7		1FH		COM31
0	1	0	0	D0	Page 4	20H	32 lines	COM32
				D1		21H		COM33
				D2		22H		COM34
				D3		23H		COM35
				D4		24H		COM36
				D5		25H		COM37
				D6		26H		COM38
				D7		27H		COM39
0	1	0	1	D0	Page 5	28H	32 lines	COM40
				D1		29H		COM41
				D2		2AH		COM42
				D3		2BH		COM43
				D4		2CH		COM44
				D5		2DH		COM45
				D6		2EH		COM46
				D7		2FH		COM47
0	1	1	0	D0	Page 6	30H	32 lines	COM48
				D1		31H		COM49
				D2		32H		COM50
				D3		33H		COM51
				D4		34H		COM52
				D5		35H		COM53
				D6		36H		COM54
				D7		37H		COM55
0	1	1	1	D0	Page 7	38H	32 lines	COM56
				D1		39H		COM57
				D2		3AH		COM58
				D3		3BH		COM59
				D4		3CH		COM60
				D5		3DH		COM61
				D6		3EH		COM62
				D7		3FH		COM63
1	0	0	0	D0	Page 8			COMS(未使用)

S0	S1	S2	S3	S4	S5	S6	S7	S8	S123	S124	S125	S126	S127	S128(未使用)	S129(未使用)	S130(未使用)	S131(未使用)										
00	01	02	03	04	05	06	07	08	08	07	06	05	04	03	02	01	00										
83	82	81	80	7F	7E	7D	7C	7B	7B	7C	7D	7E	7F	80	81	82	83										
<table border="1"> <tr> <td>1</td><td>0</td> </tr> <tr> <td>D0</td><td>D0</td> </tr> <tr> <td colspan="2">ADC</td> </tr> <tr> <td colspan="2">Column address</td> </tr> <tr> <td colspan="2">LCD OUT</td> </tr> </table>																		1	0	D0	D0	ADC		Column address		LCD OUT	
1	0																										
D0	D0																										
ADC																											
Column address																											
LCD OUT																											

Regardless of the display start line address,
 1/65duty =>64th line
 1/49duty =>48th line
 1/33duty =>32th line
 1/55duty =>54th line
 1/53duty =>52th line

● The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.

Because the display normal/reverse status, display ON/OFF

status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

● The Common Output Status Select Circuit

In the PRODUCT chips, the COM output scan direction can be selected by the common output status select command. (See Table) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Status	COM Scan Direction				
	1/65 DUTY	1/49 DUTY	1/33 DUTY	1/55 DUTY	1/53 DUTY
Normal	COM0 → COM63	COM0 → COM47	COM0 → COM31	COM0 → COM53	COM0 → COM51
Reverse	COM63 → COM0	COM47 → COM0	COM31 → COM0	COM53 → COM0	COM51 → COM0

Duty	COM dir	Common output pins							
		COM[0:15]	COM[16:23]	COM[24:26]	COM[27:36]	COM[37:39]	COM[40:47]	COM[48:63]	COMS
1/65	0				COM[0:63]				COMS
	1				COM[63:0]				COMS
1/49	0	COM[0:23]			Reserved		COM[24:47]		COMS
	1	COM[47:24]			Reserved		COM[23:0]		COMS
1/33	0	COM[0:15]			Reserved		COM[16:31]		COMS
	1	COM[31:16]			Reserved		COM[15:0]		COMS
1/55	0	COM[0:26]			Reserved		COM[27:53]		COMS
	1	COM[53:27]			Reserved		COM[26:0]		COMS
1/53	0	COM[0:25]			Reserved		COM[26:51]		COMS
	1	COM[51:26]			Reserved		COM[25:0]		COMS

● The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel.

bit	function	Status	
		"1"	"0"
D2	Booster circuit control bit	ON	OFF
D1	Voltage regulator circuit control bit (V/R circuit)	ON	OFF
D0	Voltage follower circuit control bit (V/F circuit)	ON	OFF

The Control Details of Each Bit of the Power Control Set Command

Use Settings	D2	D1	D0	Voltage booster	Voltage regulator	Voltage follower	Step-up voltage
Only the internal power supply is used(Default)	1	1	1	ON	ON	ON	Used
Only the voltage regulator circuit and the voltage follower circuit are used	0	1	1	OFF	ON	ON	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	Open

Reference Combinations

* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

● The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the LCD driver voltage V0 through the voltage regulator circuit. Because the product chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. (VREG: thermal gradients approximate -0.05%/°C)

(A) When the V0 Voltage Regulator Internal Resistors Are Used

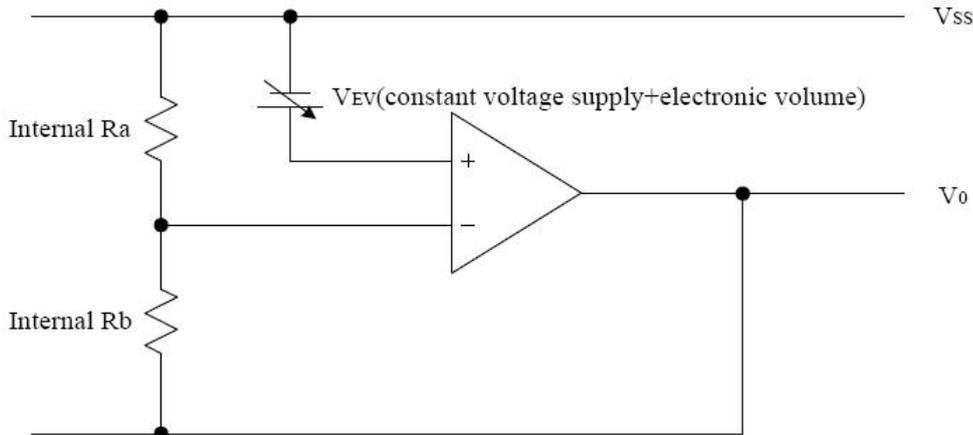
Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where $|V0| < |$

VOUT].

$$V_o = \left(1 + \frac{R_b}{R_a}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{R_b}{R_a}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG} \right]$$



VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in the following table
Condition: Ta = 25°C

Part no.	Equipment Type	Thermal Gradient	VREG
PRODUCT	Internal Power Supply	-0.05 %/°C	2.1V

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume registers. Table 10 shows the value for α depending on the electronic volume register settings.

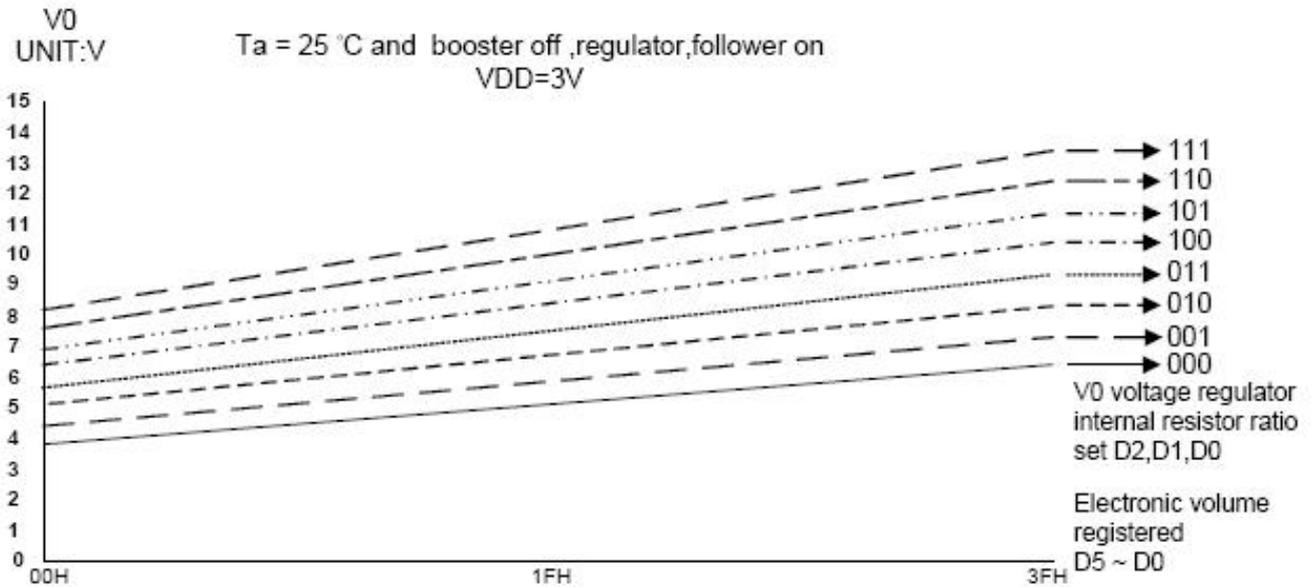
Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			⋮			⋮
			⋮			⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V0 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Register			PRODUCT
D2	D1	D0	(1) -0.05 %/°C
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

The following figures show V0 voltage measured by values of the internal resistance ratio resistor for V0 voltage adjustment and electric volume resistor for each temperature grade model.



The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volume register.

(B) When an External Resistance is Used (The V0 Voltage Regulator Internal Resistors Are Not Used) (1)

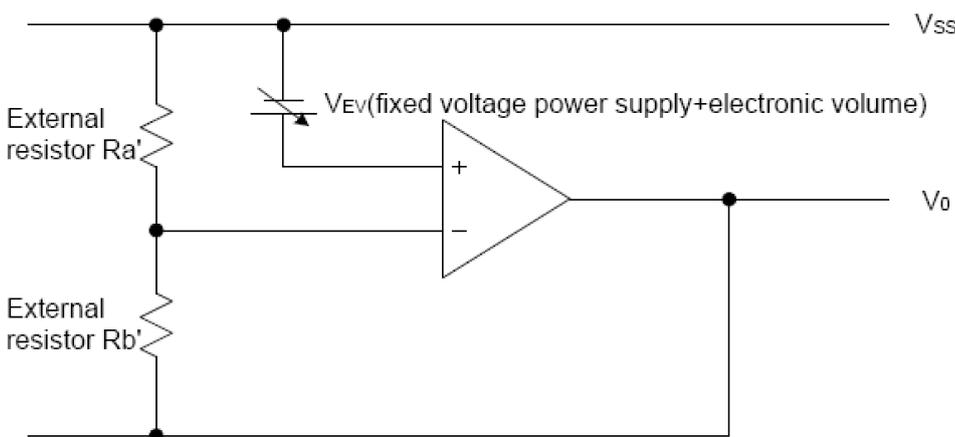
The liquid crystal power supply voltage V0 can also be set without using the V0 voltage regulator internal resistors (IRS terminal = "L") by adding resistors Ra' and Rb' between VDD and VR, and between VR and V0, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V0 through commands.

In the range where | V0 | < | VOUT |, the V0 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_0 = \left(1 + \frac{R_{b'}}{R_{a'}}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{R_{b'}}{R_{a'}}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG} \right]$$

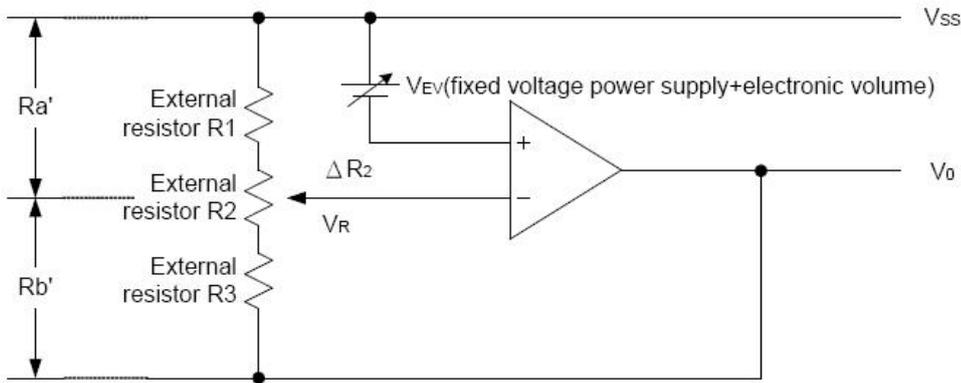


(C) When External Resistors are Used (The V0 Voltage Regulator Internal Resistors Are Not Used) (2)

When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V0. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V0 by commands to adjust the liquid crystal display brightness.

In the range where | V0 | < | VOUT | the V0 voltage can be calculated by equation C-1 below based on the R1 and R2 (variable resistor) and R3 settings, where R2 can be subjected to fine adjustments (Δ R2).

$$\begin{aligned}
 V_0 &= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \cdot V_{EV} \\
 &= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG} \\
 \left[\because V_{EV} &= \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG} \right]
 \end{aligned}$$



- * When the V0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.
- * The VR terminal is enabled only when the V0 voltage regulator internal resistors are not used (i.e. the IRS terminal = “L”). When the V0 voltage regulator internal resistors are used (i.e. when the IRS terminal = “H”), then the VR terminal is left open.
- * Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

● The Internal Power Supply Shutdown Command Sequence

The sequence shown in the following figures is recommended for shutting down the internal power supply, first placing the internal power supply in power saver mode and then turning the internal power supply OFF. The power consumption can be reduced by this sequence. Please refer to the “Sleep Mode Set” section for the detailed power saving information.

Sequence	Details	Command address									
	(Command, status)	D7	D6	D5	D4	D3	D2	D1	D0		
Step1	Display OFF	1	0	1	0	1	1	1	0	Power saver commands (compound)	
Step2	Display all points ON	1	0	1	0	0	1	0	1		
End	Internal power supply OFF										

● The Reset Circuit

When the /RES input comes to the “L” level, these LSIs return to the default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC command D0 = “L”)
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. 4-line SPI interface internal register data clear
6. LCD power supply bias rate:
 - 1/65 DUTY = 1/9 bias
 - 1/49, 1/55, 1/53 DUTY = 1/8 bias
 - 1/33 DUTY = 1/6 bias
7. Power saving clear
8. V0 voltage regulator internal resistors Ra and Rb separation
9. Output conditions of SEG and COM terminals
 - SEG=VSS, COM=VSS
10. Read modify write OFF
11. Display start line set to first line
12. Column address set to Address 0

13. Page address set to Page 0
14. Common output status normal
15. V0 voltage regulator internal resistor ratio set mode clear
16. Electronic volume register set mode clear Electronic volume register:
(D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0)
17. Test mode clear

On the other hand, when the reset command is used, the above default settings from 11 to 17 are only executed. When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the /RES terminal. After the initialization, each input terminal should be controlled normally.

Moreover, when the control signal from the MPU is in the high impedance, an over current may flow to the IC. After applying a current, it is necessary to take proper measures to prevent the input terminal from getting into the high impedance state.

If the internal liquid crystal power supply circuit is not used on the product, it is necessary that /RES is "H" when the external liquid crystal power supply is turned on. This IC has the function to discharge V0 when /RES is "L," and the external power supply short-circuits to VSS when /RES is "L." This means that an internal resistor is connected between VSS and V0.

While /RES is "L," the oscillator works but the display timing generator stops, and the CL, FR and /DOF terminals are fixed to "H." The terminals D0 to D7 are not affected. The VSS level is output to the SEG and COM output terminals after a successful hardware reset.

▼ **Command**

The ST7565R identify the data bus signals by a combination of A0, /RD (E), /WR(R/W) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.

In the 8080 MPU interface, commands are launched by inputting a low pulse to the RD terminal for reading, and inputting a low pulse to the /WR terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an “H” signal is input to the R/W terminal and placed in a write mode when a “L” signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read /RD (E) becomes “1(H)”. In the explanations below the commands are explained using the 8080 Series MPU interface as the example.

When the 4-line SPI interface is selected, the data is input in sequence starting with D7.

<Explanation of Commands>

● **Display ON/OFF**

This command turns the display ON and OFF.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, Sleep mode is entered. See the section on the Sleep Mode Set for details.

● **Display Start Line Set**

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in “The Line Address Circuit”.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	1	0	0	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

● **Page Address Set**

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
											↓
							0	1	1	1	7
							1	0	0	0	8

● **Column Address Set**

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in “The Column Address Circuit,” for details.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Page address
High bits→	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits→							0	A3	A2	A1	A0	0	0	0	0	0	0	1	0	0
												0	1	1	1	1	1	1	1	1
												1	0	0	0	0	0	0	0	128(未使用)
												1	0	0	0	0	0	0	1	129(未使用)
												1	0	0	0	0	0	1	0	130(未使用)
												1	0	0	0	0	0	1	1	131(未使用)

● Status Read

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	BUSY = 1: it indicates that either processing is occurring internally or a reset condition is in process. BUSY = 0: A new command can be accepted, if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n SEG n) 1: Normal (column address n SEG n) (The ADC command switches the
ON/OFF	ON/OFF: indicates the display ON/OFF state. 1: Display ON 0: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a /RES signal or because of a reset command. 0: Operating state 1: Reset in progress

● Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by “1” after the write, the MPU can write the display data.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

● Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by “1” after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in “Display Data RAM” for the explanation of accessing the internal registers. When the 4-line SPI interface is used, reading of the display data becomes unavailable.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

● ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit for the detail. Increment of the column address (by “1”) accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

● **Display Normal/Reverse**

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data “H” LCD ON voltage (normal)
										1	RAM Data “L” LCD ON voltage (reverse)

● **Display All Points ON/OFF**

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in sleep mode. For details, see the Sleep Mode Set section.

● **LCD Bias Set**

This command selects the voltage bias ratio required for the liquid crystal display.

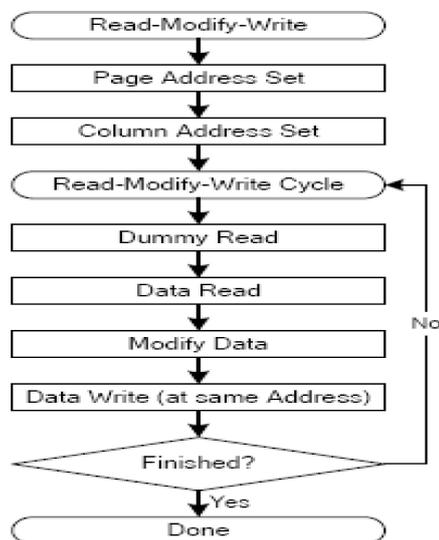
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Select Status				
											1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

● **Read-Modify-Write**

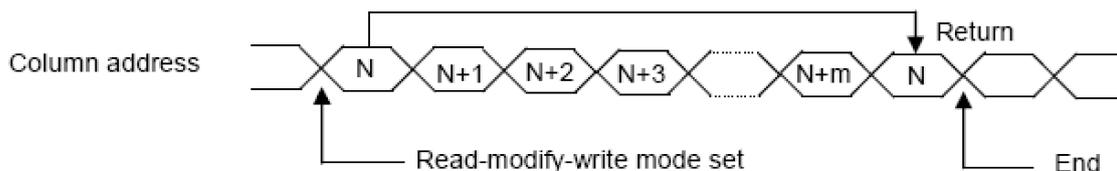
This command is used paired with the “END” command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the Read-Modify-Write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.



Command Sequence For read modify write



● **End**

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

● **Reset**

This command initializes the display start line, the column address, the page address, the common output mode, the V0 voltage regulator internal resistor ratio, the electronic volume, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in “Reset” for details.

The reset operation is performed after the reset command is entered.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the /RES terminal. The reset command must not be used instead.

● **Common Output Mode Select**

This command can select the scan direction of the COM output terminal. For details, see the function explanation in “Common Output Mode Select Circuit.”

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Select Mode					
												1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0→ COM63	COM0→ COM47	COM0→ COM31	COM0→ COM53	COM0→ COM51
											Reverse	COM63→ COM0	COM47→ COM0	COM31→ COM0	COM53→ COM0	COM51→ COM0

* Disabled bit

● **Power Controller Set**

This command sets the power supply circuit functions. See the function explanation in “The Power Supply Circuit,” for details

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
											Booster circuit: ON
											Voltage regulator circuit: OFF
											Voltage regulator circuit: ON
0	1	0									Voltage follower circuit: OFF
											Voltage follower circuit: ON

● **V0 Voltage Regulator Internal Resistor Ratio Set**

This command sets the V0 voltage regulator internal resistor ratio. For details, see the function explanation is “The Voltage Regulator circuit” and table 11 .

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
0	1	0									Large

● **The Electronic Volume (Double Byte Command)**

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

● **The Electronic Volume Mode Set**

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

● **Electronic Volume Register Set**

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V0 assumes one of the 64 voltage levels.

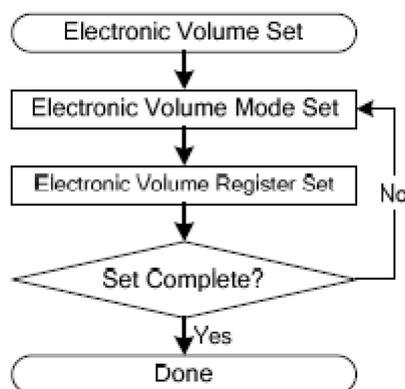
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	V0		
0	1	0	*	*	0	0	0	0	0	1	Small		
			*	*	0	0	0	0	1	0			
			*	*	0	0	0	0	1	1			
													▶
			*	*	1	1	1	1	1	0			↓
			*	*	1	1	1	1	1		Large		

* Inactive bit (set "0")

When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

● **The Electronic Volume Register Set Sequence**



● **Sleep Mode Set (Double Byte Command)**

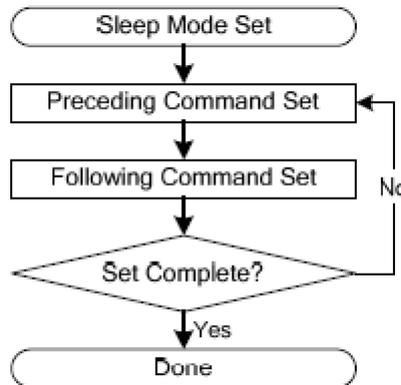
This command is a two byte command used as a pair with preceding command and following command, and both commands must be issued one after the other.

This command stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

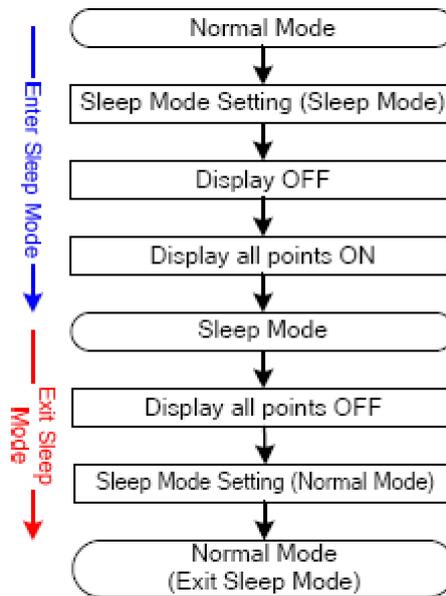
1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VSS level.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
Preceding Command	0	1	0	1	0	1	0	1	1	0	0	Sleep Mode
										1	0	
Following Command										0	0	

* Disabled bit (set "0")



In the sleep mode, the MPU is still able to access the display data RAM. Refer to figure 28 for sleep mode sequence.



• The Booster Ratio (Double Byte Command)

This command makes it possible to select step-up ratio. It is used when the power control set have turn on the internal booster circuit. This command is a two byte command used as a pair with the booster ratio select mode set command and the booster ratio register set command, and both commands must be issued one after the other.

• Booster Ratio Select Mode Set

When this command is input, the Booster ratio register set command becomes enabled. Once the booster ratio select mode has been set, no other command except for the booster ratio register command can be used. Once the booster ratio register set command has been used to set data into the register, then the booster ratio select mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

• Boostet Ratio Register Set

By using this command to set two bits of data to the booster ratio register, it can be select what kind of the booster ratio can be used.

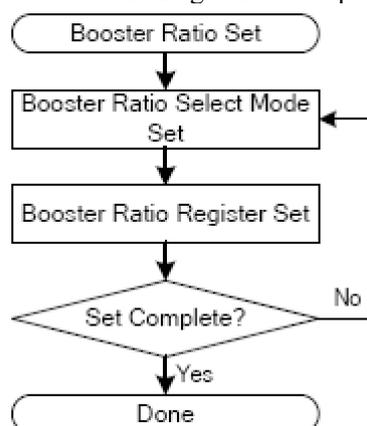
When this command is input, the booster ratio select mode is released after the booster ratio register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Booster ratio select
0	1	0	*	*	*	*	*	*	0	0	2x,3x,4x
			*	*	*	*	*	*	0	1	5x
			*	*	*	*	*	*	1	1	6x

* Inactive bit (set "0")

When the booster ratio select function is not used, set this to (0, 0) 2x,,3x,4x step-up mode

The booster ratio Register Set Sequence

● **NOP**

Non-Operation Command

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

● **Test**

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a “L” signal to the /RES input by the reset command or by using an NOP.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	1	*	*

* Inactive bit

Note: The ST7565R maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the ST7565R . Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

▼ Table of Commands

(Note) *: ignored data

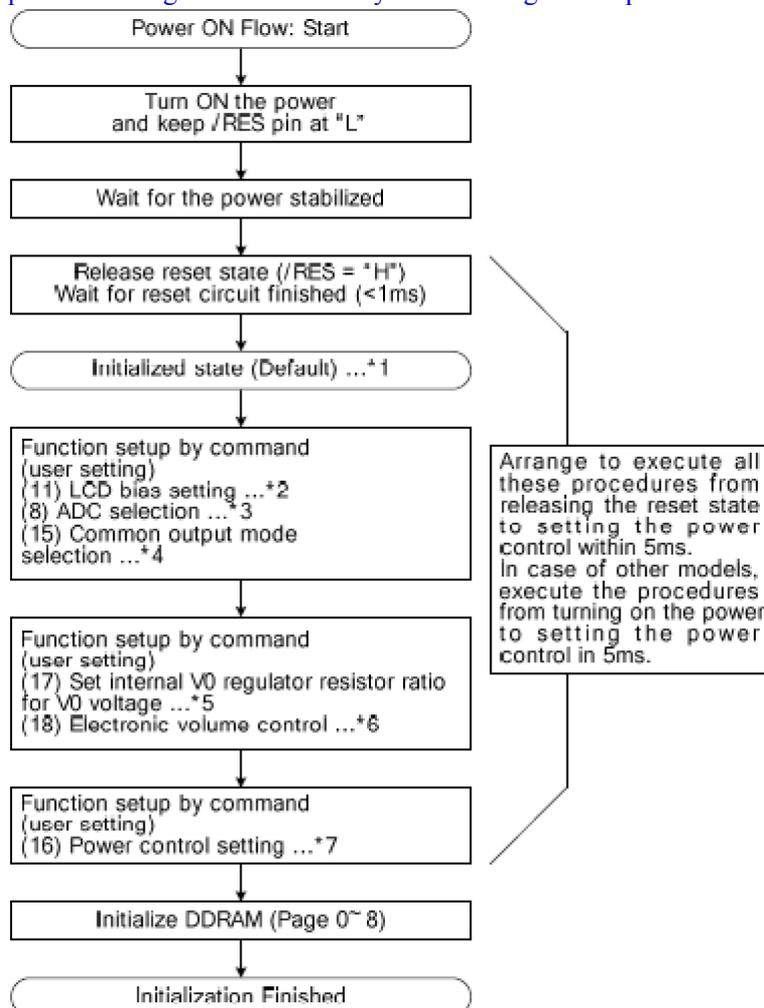
Command	Command Code										Function	
	A0	/RD	/WR	D0	D1	D2	D3	D4	D5	D6		D7
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address					0	Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0	1	0	0	0	0	1	Most significant column address			0	Sets the most significant 4 bits of the display RAM column address.
				0	0	0	0	Least significant column address			0	Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data							0	Writes to the display RAM
(7) Display data read	1	0	1	Read data							0	Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/reverse	0	1	0	1	0	1	0	0	1	1	0	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias
(12) Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode		0	Select internal power supply operating mode
(17) V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio		0	Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1	0	0	0	0	0	0	1	Set the V0 output voltage electronic volume register
				0	0	Electronic volume value					0	
(19) Sleep mode set	0	1	0	1	0	1	0	1	1	0	0	0: Sleep mode, 1: Normal mode
				*	*	*	*	*	*	0	0	
(20) Booster ratio set	0	1	0	1	1	1	1	1	0	0	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
				0	0	0	0	0	0	0	step-up value	
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

▼ Command Description

● Instruction Setup: Reference

(A) Initialization

I. When the built-in power is being used immediately after turning on the power:



* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; resetting circuit

*2: Command description; LCD bias setting

*3: Command description; ADC selection

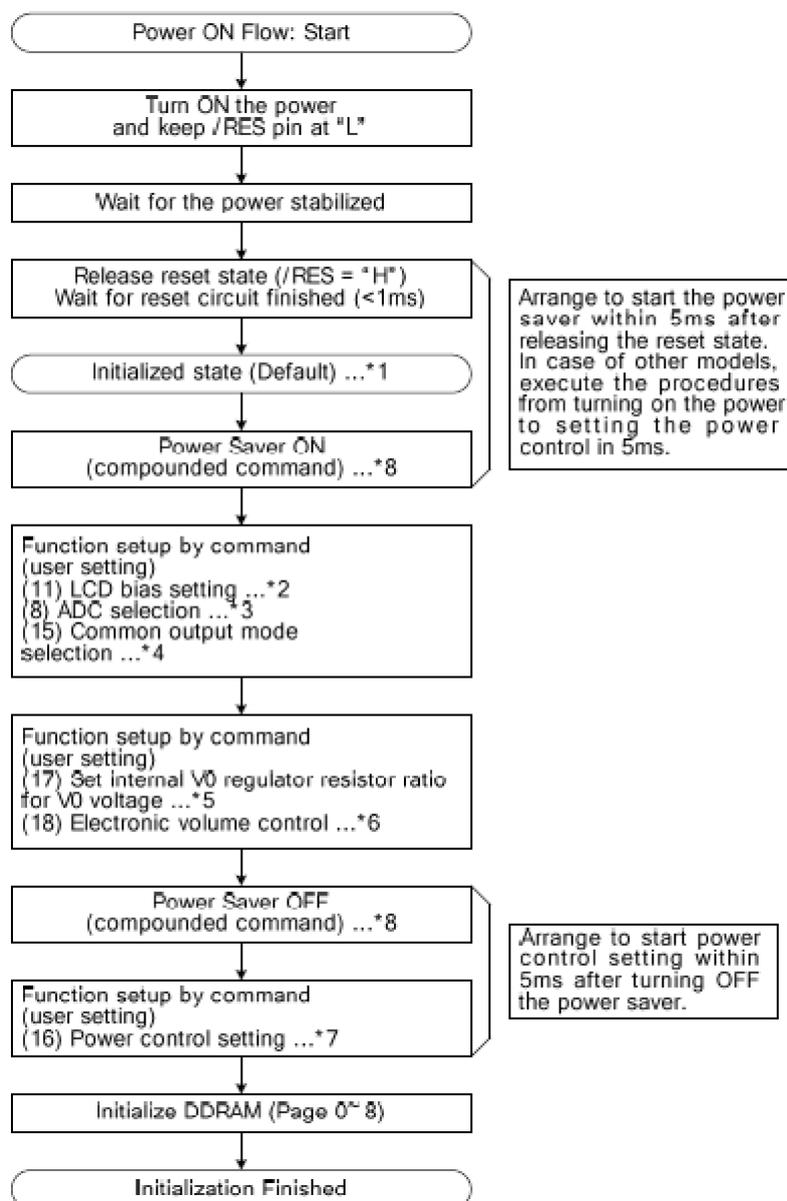
*4: Command description; Common output state selection

*5: Description of functions; Power circuit & Command description; Setting the built-in resistance ratio for regulation of the V0 voltage

*6: Description of functions; Power circuit & Command description; Electronic volume control

*7: Description of functions; Power circuit & Command description; Power control setting

II. When the built-in power is not being used immediately after turning on the power:



* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; resetting circuit

*2: Command description; LCD bias setting

*3: Command description; ADC selection

*4: Command description; Common output state selection

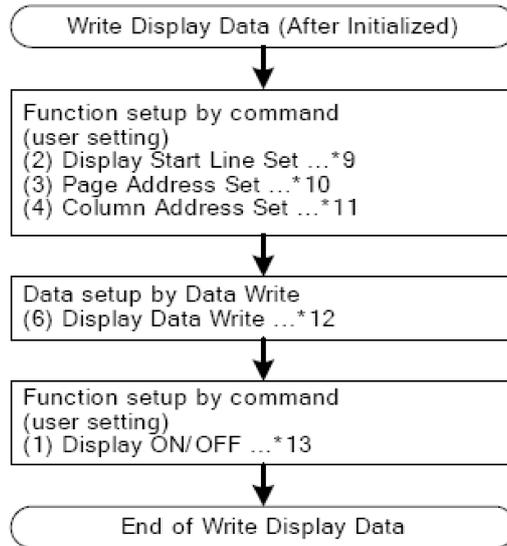
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance ratio for regulation of the V0 voltage

*6: Description of functions; Power circuit & Command description; Electronic volume control

*7: Description of functions; Power circuit & Command description; Power control setting

*8: Command description; Sleep mode (multiple commands)

(2) Data Display

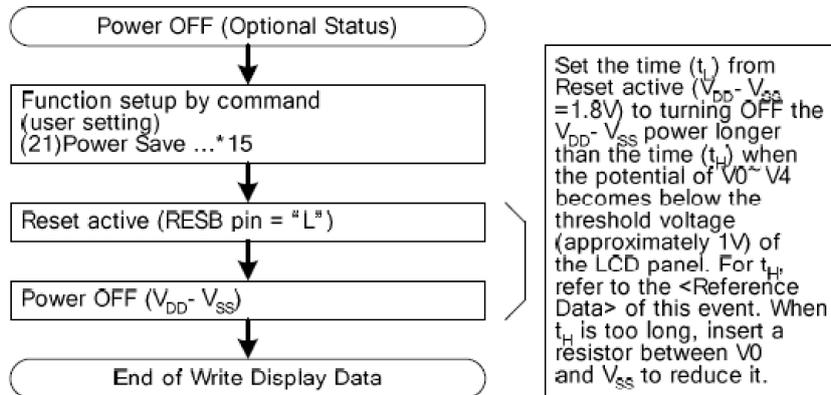


Notes: Reference items

- *9: Command Description; Display start line set
- *10: Command Description; Page address set
- *11: Command Description; Column address set
- *12: Command Description; Display data write
- *13: Command Description; Display ON/OFF

Avoid displaying all the data at the data display start (when the display is ON) in white.

(3) Power OFF *14

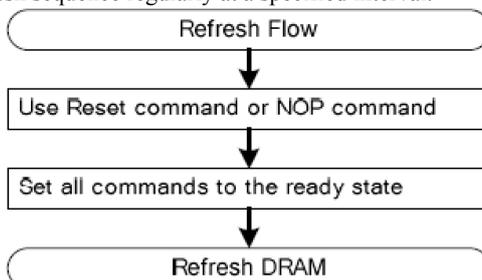


Notes: Reference items

- *14: The logic circuit of this IC's power supply VDD - VSS controls the driver of the LCD power supply VSS -V0. So, if the power supply VDD - VSS is cut off when the LCD power supply VSS -V0 has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:
 - After turning off the internal power supply, make sure that the potential V0 ~ V4 has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (VDD - VSS). 6. Description of Function, 6.7 Power Circuit
- *15: After inputting the power save command, be sure to reset the function using the /RES terminal until the power supply VDD - VSS is turned off. 7. Command Description (19) Sleep Mode Set
- *16: After inputting the power save command, do not reset the function using the /RES terminal until the power supply VDD - VSS is turned off. 7. Command Description (19) Sleep Mode Set

● Refresh

It is recommended to turn on the refresh sequence regularly at a specified interval.



■ DISPLAY DATA RAM ADDRESS MAP

Common output mode select						SEG														COM		
C0H			C8H			SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	...	SEG120	SEG121	SEG122	SEG123	SEG124		SEG125	SEG126
Line Address	Page Address	Data	Line Address	Page Address	Data																
63	07	D7	0	00	D0	<p style="text-align: center;">LCD Panel 128*64 DOTS</p> <p>左上角点,坐标(0,0) 右上角点,坐标(128,0)</p>																COM63
62		D6	1		D1																	COM62
61		D5	2		D2																	COM61
60		D4	3		D3																	COM60
59		D3	4		D4																	COM59
58		D2	5		D5																	COM58
57		D1	6		D6																	COM57
56	D0	7	D7	COM56																		
55	06	D7	8	01	D0																	COM55
54		D6	9		D1																	COM54
53		D5	10		D2																	COM53
52		D4	11		D3																	COM52
51		D3	12		D4																	COM51
50		D2	13		D5																	COM50
49		D1	14		D6																	COM49
48	D0	15	D7	COM48																		
47	05	D7	16	02	D0																	COM47
46		D6	17		D1																	COM46
45		D5	18		D2																	COM45
44		D4	19		D3																	COM44
43		D3	20		D4																	COM43
42		D2	21		D5																	COM42
41		D1	22		D6																	COM41
40	D0	23	D7	COM40																		
...																
23	02	D7	40	05	D0	COM23																
22		D6	41		D1	COM22																
21		D5	42		D2	COM21																
20		D4	43		D3	COM20																
19		D3	44		D4	COM19																
18		D2	45		D5	COM18																
17		D1	46		D6	COM17																
16	D0	47	D7	COM16																		
15	01	D7	48	06	D0	COM15																
14		D6	49		D1	COM14																
13		D5	50		D2	COM13																
12		D4	51		D3	COM12																
11		D3	52		D4	COM11																
10		D2	53		D5	COM10																
9		D1	54		D6	COM9																
8	D0	55	D7	COM8																		
7	00	D7	56	07	D0	COM7																
6		D6	57		D1	COM6																
5		D5	58		D2	COM5																
4		D4	59		D3	COM4																
3		D3	60		D4	COM3																
2		D2	61		D5	COM2																
1		D1	62		D6	COM1																
0	D0	63	D7	COM0																		

131	0	:	120	:
130	1		121	
129	2		122	
128	3		123	
127	4		124	
126	5		125	
125	6		126	
124	7		127	
A1H	A0H	ADC select (Column Addresses)		

■ RELIABILITY

▼ Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 96hrs	----
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C 96hrs	----
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	+75°C 96hrs	----
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	-25°C 96hrs	----
5	High temperature / Humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	50 °C , 90%RH 48 hrs	MIL-202E-103B JIS-C5023
6	High temperature / Humidity operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40°C 90 %RH 48 hrs	MIL-202E-103B JIS-C5023
7	Temperature cycle	Endurance test applying the low and high temperature cycle. $\begin{array}{ccccccc} -25^{\circ}\text{C} & \rightleftharpoons & 25^{\circ}\text{C} & \rightleftharpoons & +75^{\circ}\text{C} \\ 30\text{min.} & \xleftarrow{\hspace{1cm}} & 5\text{min.} & \xrightarrow{\hspace{1cm}} & 30\text{min.} \\ & \xrightarrow{\hspace{1.5cm}} & & \xleftarrow{\hspace{1.5cm}} & \\ & \text{1 cycle} & & & \end{array}$	-25°C / 75°C 10 cycles	----
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz → 1.5mmp-p 22~500Hz → 1.5G Total 0.5hrs	MIL-202E-201A JIS-C5025 JIS-C7022-A-10
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 11 msdc 3 times of each direction	MIL-202E-213B
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115 mbar 40 hrs	MIL-202E-105C
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V , RS=1.5 kΩ CS=100 pF 1 time	MIL-883B-3015.1

*** Supply voltage for logic system = 3.3V. Supply voltage for LCD system = Operating voltage at 25°C.

▼ Failure Judgment Criterion

Criterion Item	Test Item No.											Failure Judgment Criterion	
	1	2	3	4	5	6	7	8	9	10	11		
Basic specification													Out of the Basic Specification
Electrical characteristic													Out of the DC and AC Characteristic
Mechanical characteristic													Out of the Mechanical Specification Color change : Out of Limit Apperance Specification
Optical characteristic													Out of the Apperance Standard

■ INSPECTION CRITERIA

see :Q/XRD0002-05

■ PRECAUTIONS FOR USING LCD MODULES

▼ Handling Precautions

- (1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.
- (2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- (3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- (4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- (5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents :
 - Isopropyl alcohol
 - Ethyl alcohol
- (6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
 - Water
 - Ketoses
 - Aromatic solvents
- (7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

■ USING LCD MODULES

▼ Liquid Crystal Display Modules

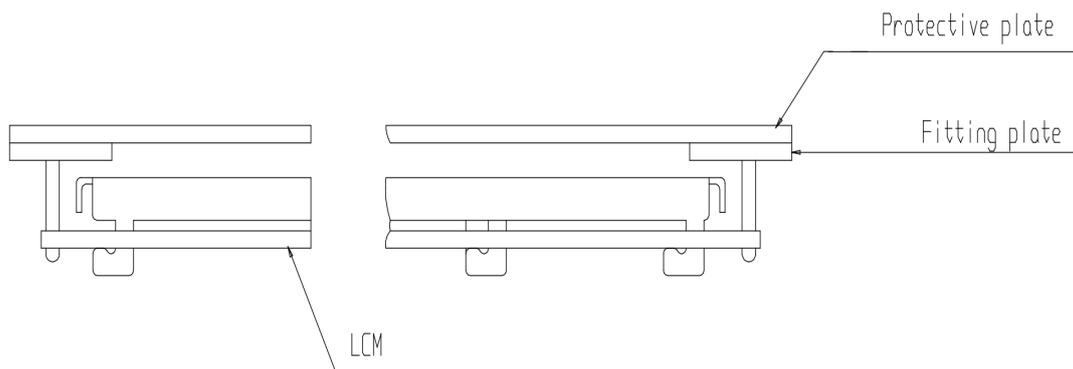
LCD is composed of glass and polarizer. Pay attention to the following items when handling.

- (1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.
- (2) Do not touch, push or rub the exposed polarizer with anything harder than an HB pencil lead (glass, tweezers, etc.).
- (3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropylalcohol.
- (4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzine. Do not scrub hard to avoid damaging the display surface.
- (5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.
- (6) Avoid contacting oil and fats.
- (7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming in contact with room temperature air.
- (8) Do not put or attach anything on the display area to avoid leaving marks on.
- (9) Do not touch the display with bare hands. This will stain the display area and degrade insulation between terminals (some cosmetics are determined to the polarizers).
- (10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

▼ Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

- (1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



- (2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ± 0.1 mm.

▼ Precaution for Handling LCD Modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

- (1) Do not alter, modify or change the shape of the tab on the metal frame.
- (2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
- (3) Do not damage or modify the pattern writing on the printed circuit board.

- (4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.
- (5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
- (6) Do not drop, bend or twist LCM.

▼ Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

- (1) Make certain that you are grounded when handling LCM.
- (2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.
- (3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.
- (4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.
- (5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.
- (6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

▼ Precaution for soldering to the LCM

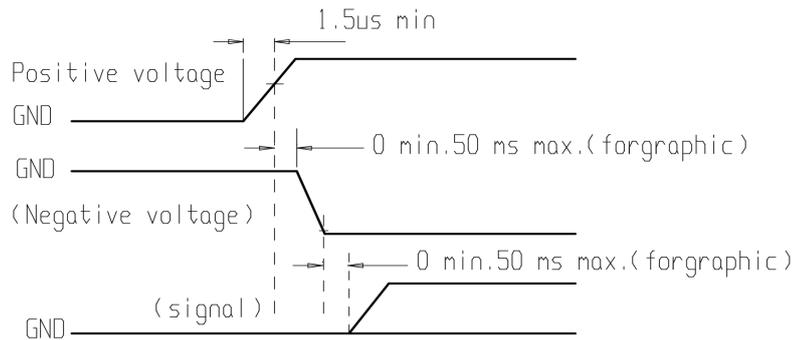
- (1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.
 - Soldering iron temperature : $280^{\circ}\text{C} \pm 10^{\circ}\text{C}$.
 - Soldering time : 3-4 sec.
 - Solder : eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

- (2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.
- (3) When remove the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

▼ Precautions for Operation

- (1) Viewing angle varies with the change of liquid crystal driving voltage (VO). Adjust VO to show the best contrast.
- (2) Driving the LCD in the voltage above the limit shortens its life.
- (3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.
- (4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.
- (5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it must be used under the relative condition of 40°C , 50% RH.
- (6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



▼ Storage

When storing LCD's as spares for some years, the following precaution are necessary.

- (1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.
- (2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.
- (3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)
- (4) Environmental conditions :
 - Do not leave them for more than 168hrs. at 80°C.
 - Should not be left for more than 48hrs. at -30°C.

▼ Safety

- (1) It is recommended to crush damaged or unnecessary LCD's into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2) If any liquid out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

▼ Limited Warranty

Unless agreed between X.R.D and customer, X.R.D will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with X.R.D LCD acceptance standards (copies available upon request) for a period of one year from date of shipments.

Cosmetic/visual defects must be returned to X.R.D within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of X.R.D limited to repair and/or replacement on the terms set forth above. X.R.D will not be responsible for any subsequent or consequential events.

▼ Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet's, conductors and terminals.

